

MODEL NAME : *PLW00*

PCB NO : *LA-7452P*

BOM P/N : *TBD*
TBD

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Schematic Document

Breitling (Huron River)

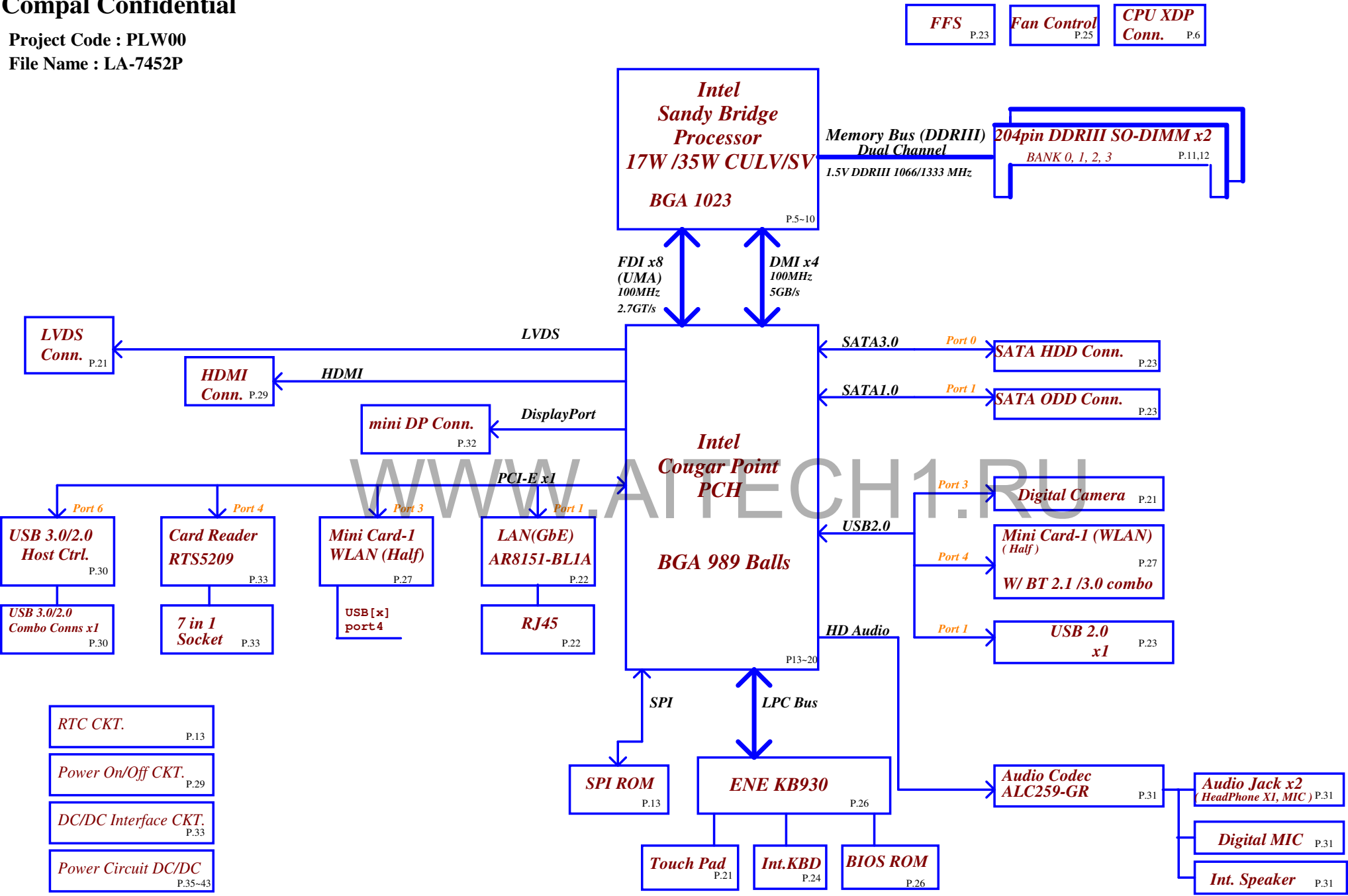
Sandy Bridge (BGA) + Cougar Point (standard)

DISCRETE VGA N12P-GV-S-A1 (optimus)

2011-07-12

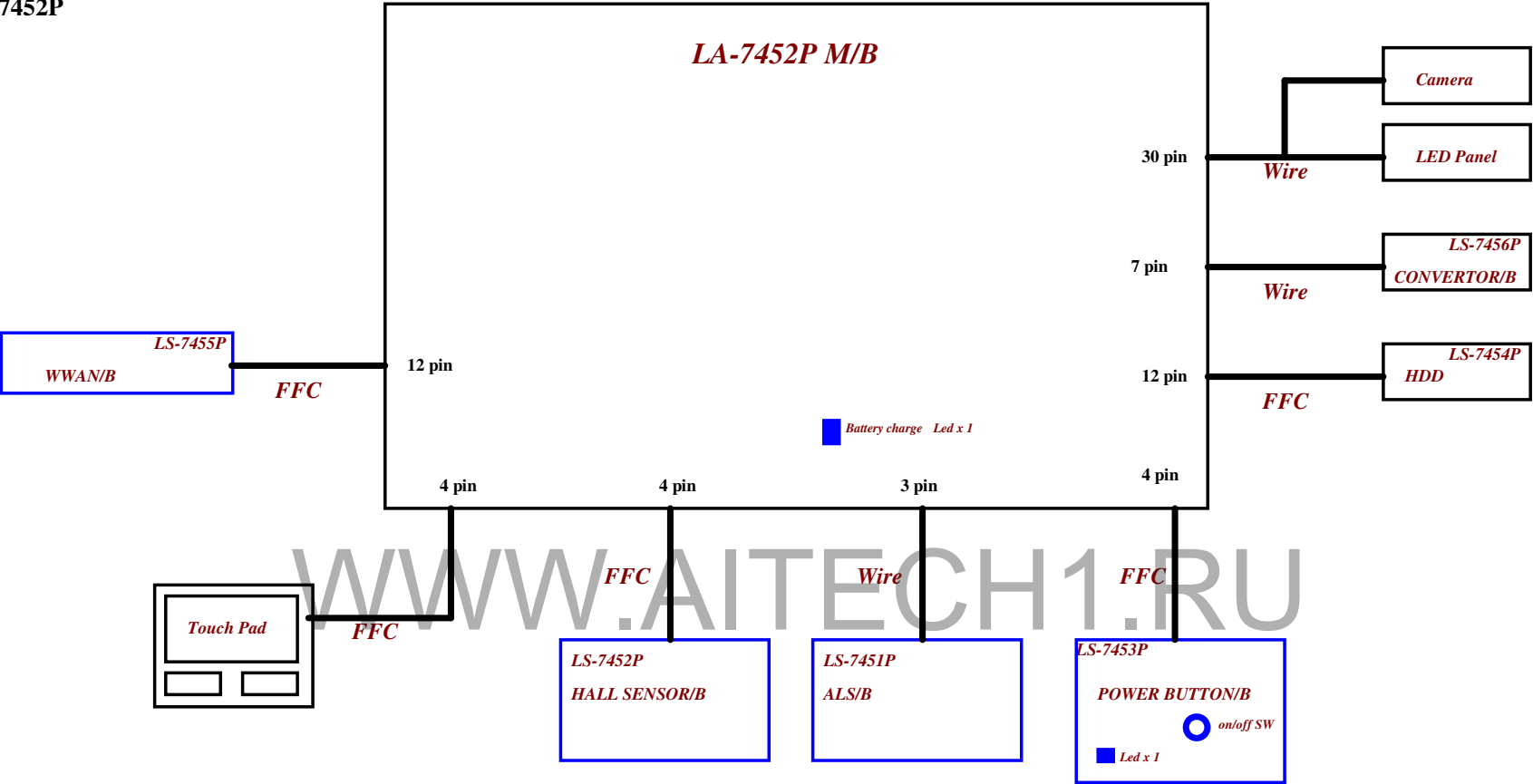
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Project Code : PLW00
File Name : LA-7452P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	A.0
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	SODIMM	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930												
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH											V	
MEM_SMBCLK MEM_SMBDATA	PCH				V	V		V					V

Link

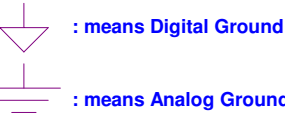
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

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SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

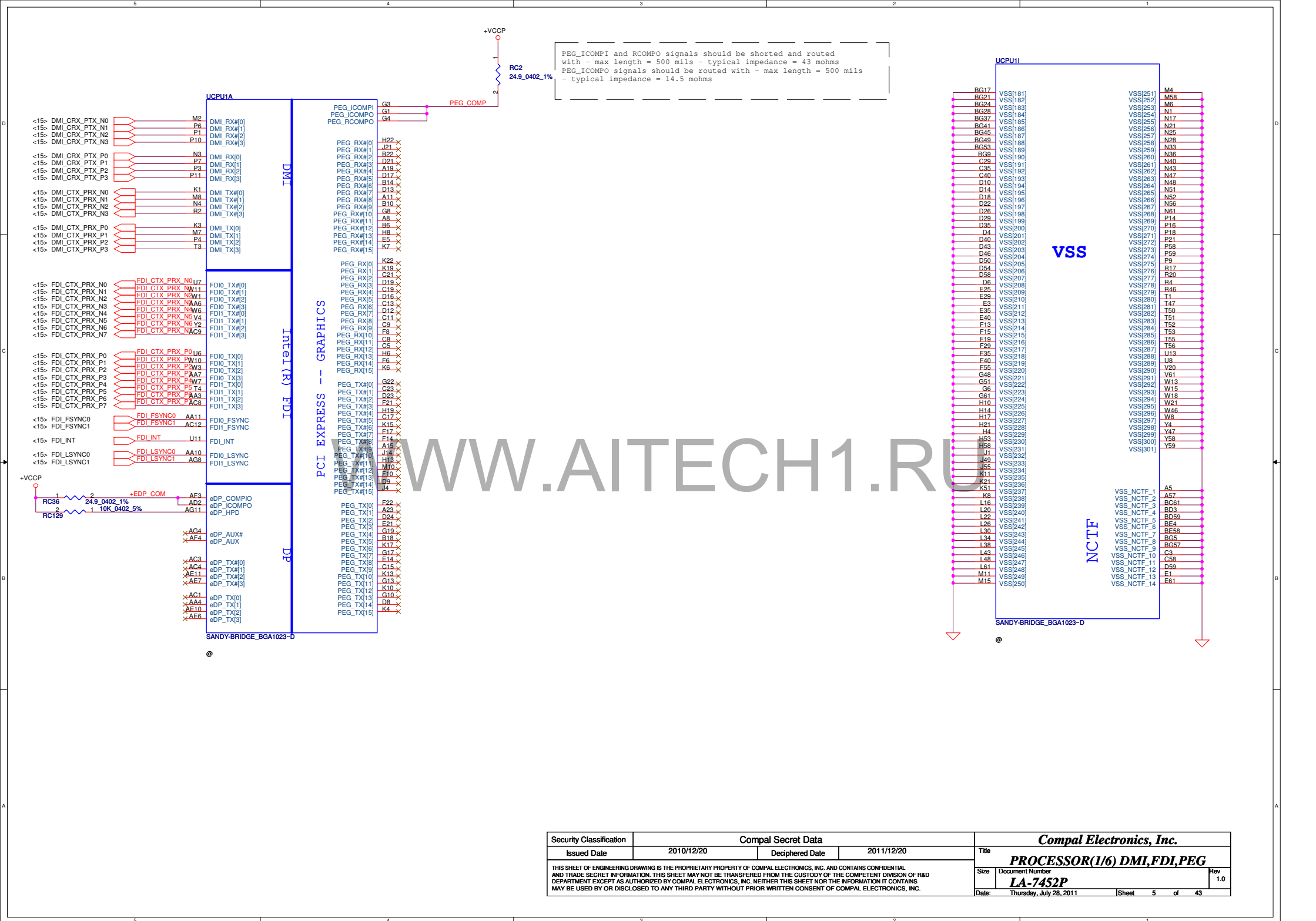
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

Symbol Note :

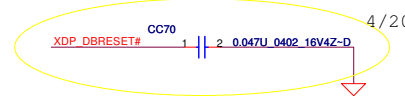
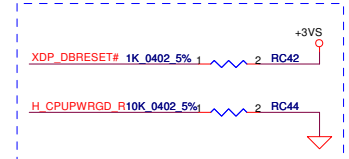
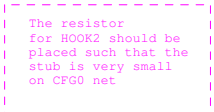
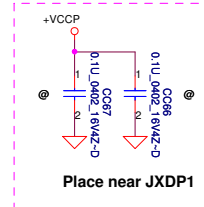


CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

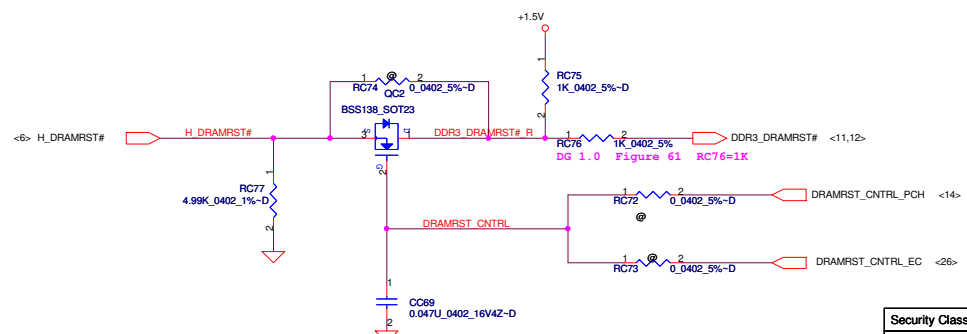
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				PROCESSOR(2/6) PM,XDP,CLK	
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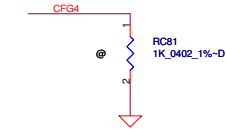
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CFG2

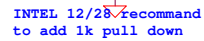
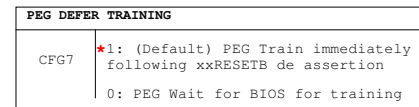
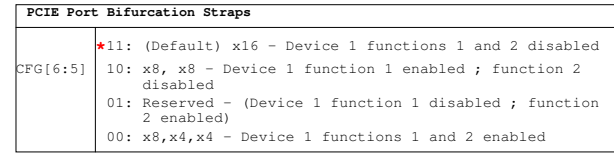
RC78
1K_0402_1%-D

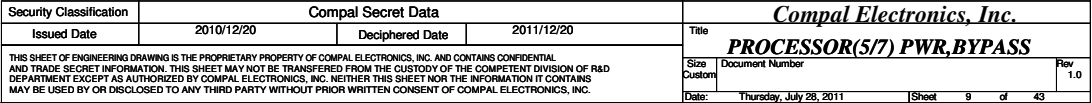
16x Lane Reversal - CFG2 is for the 16x

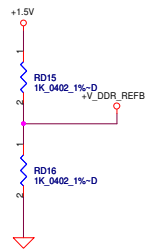
CFG2	<p>★1:(Default) Normal Operation; Lane # definition matches socket pin map definition</p> <p>0:Lane Reversed</p>
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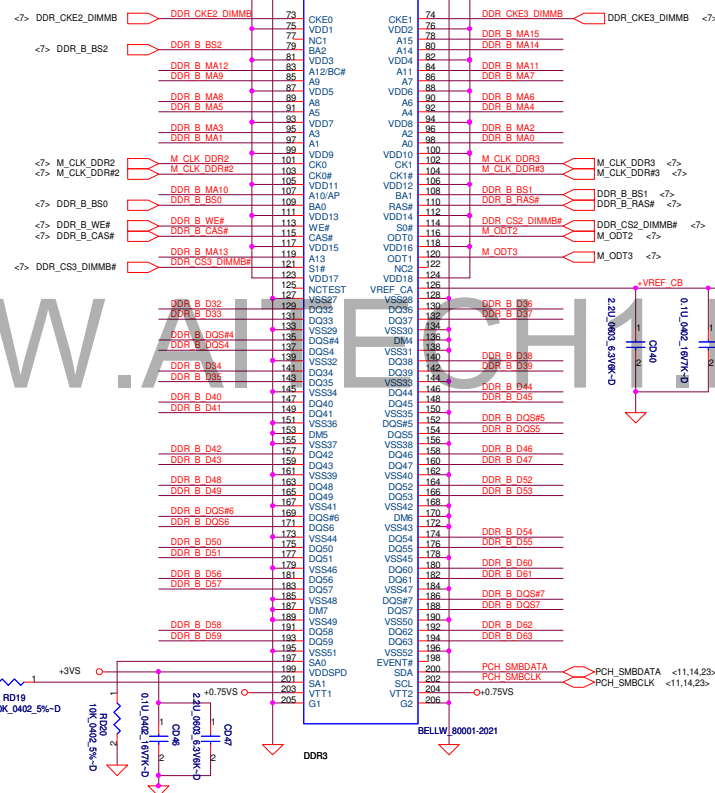
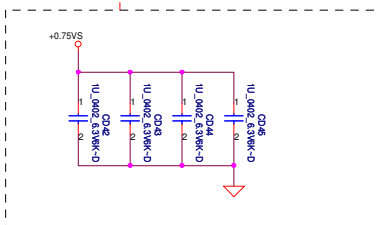
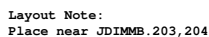
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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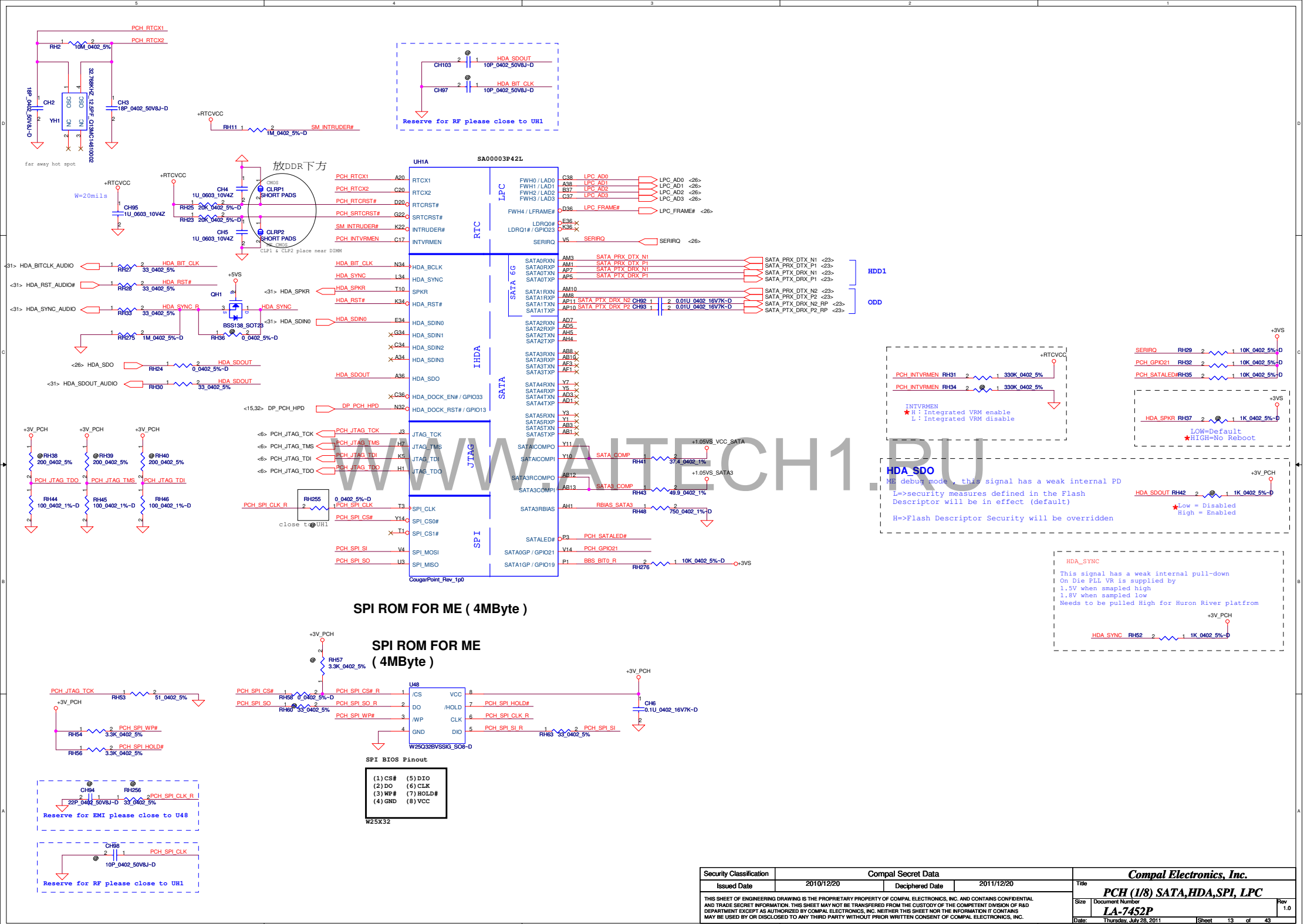


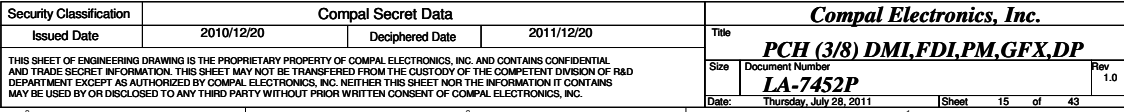


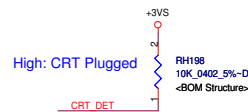
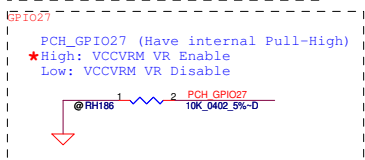
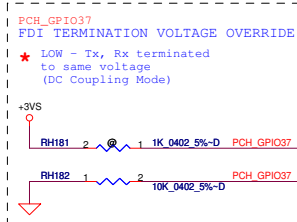
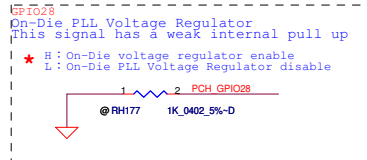
All VREF traces should have 10 mil trace width



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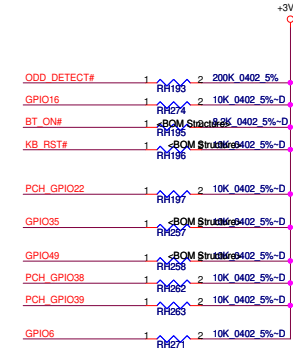
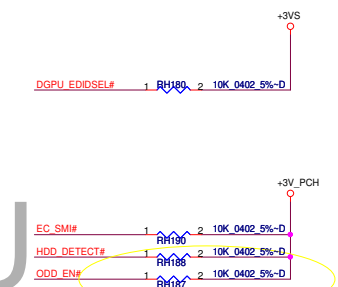
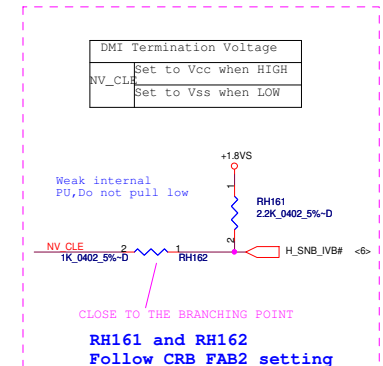
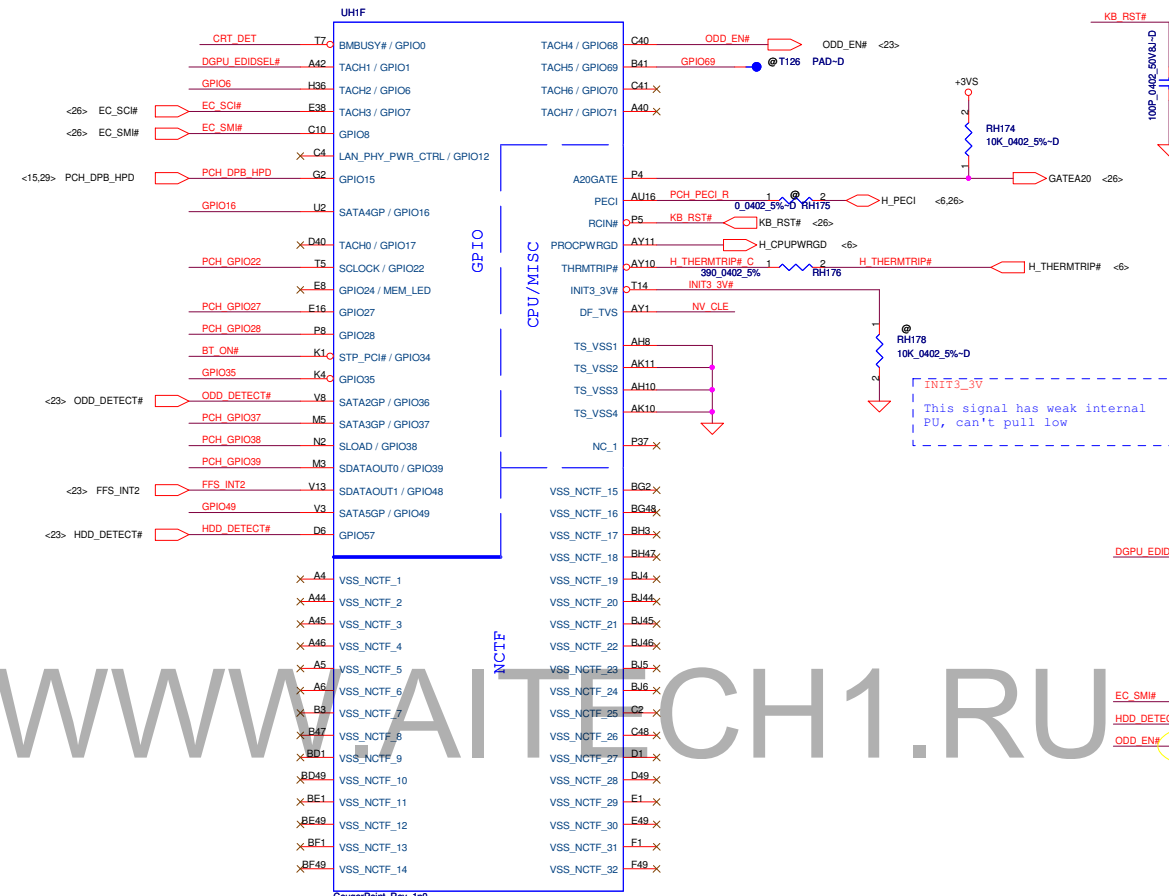




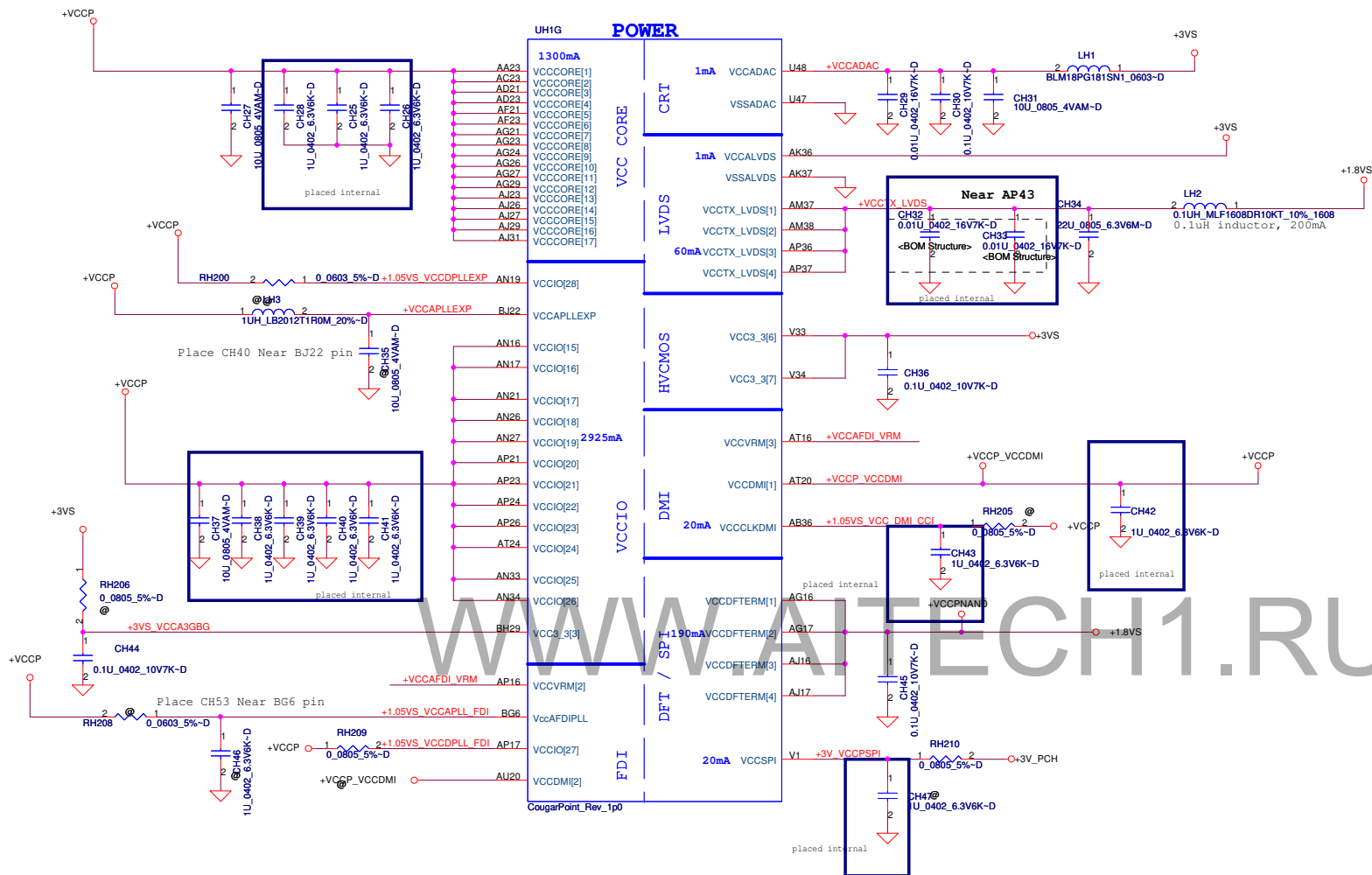
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

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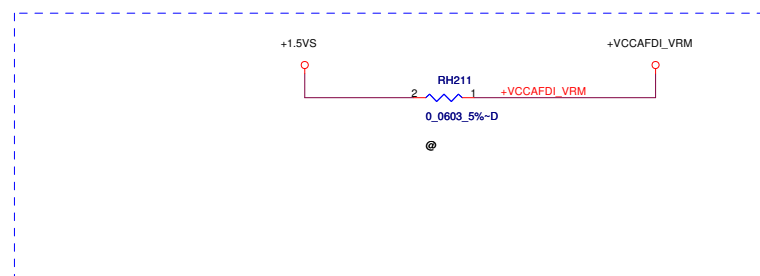


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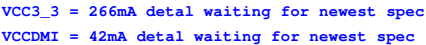


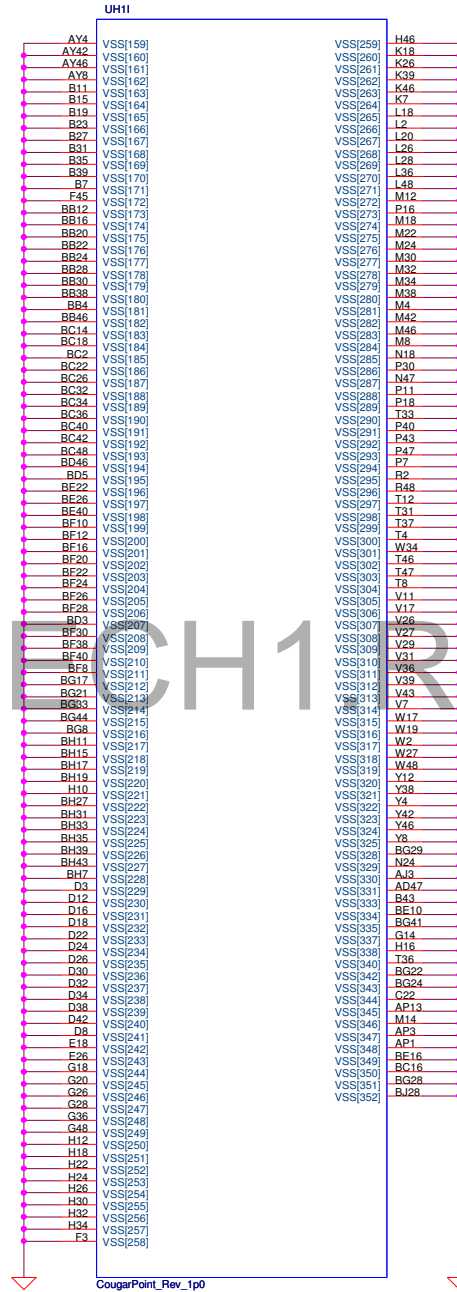
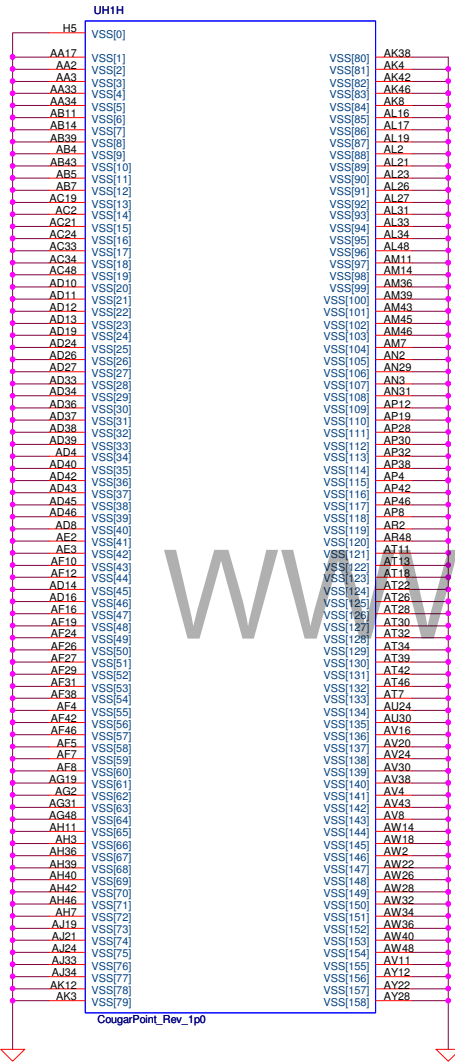
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLL B	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec



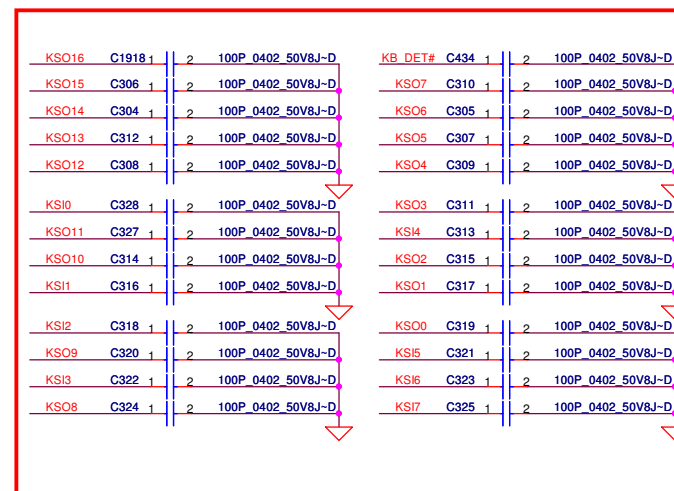
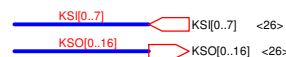
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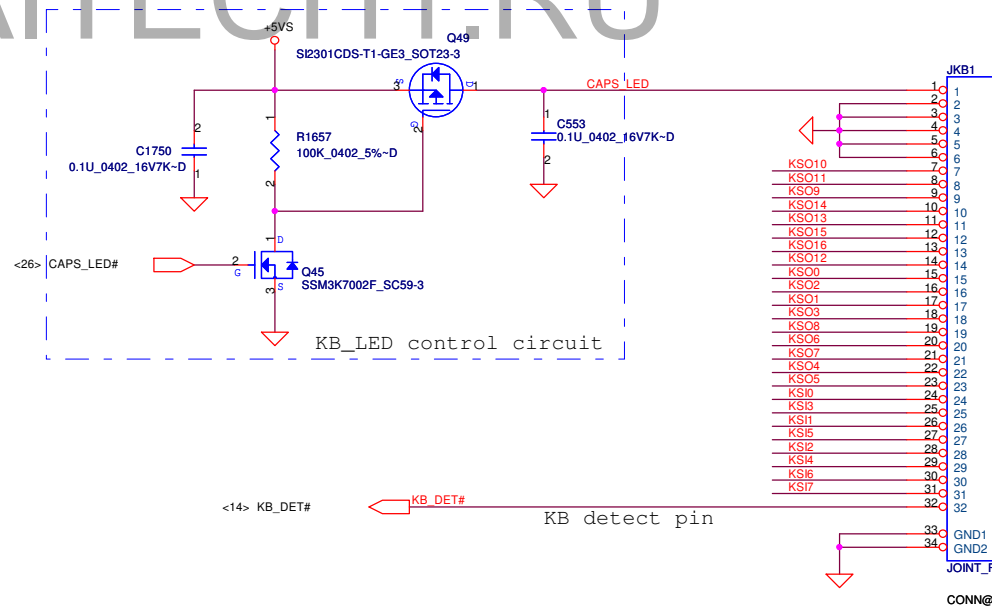
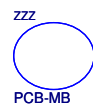
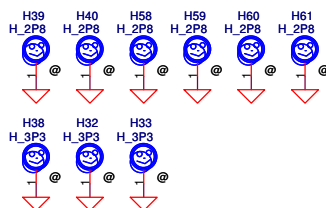


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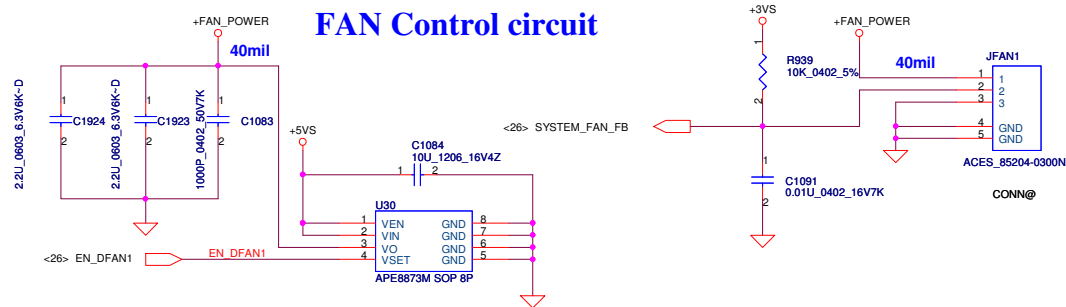
Power Button



INT_KBD Conn.

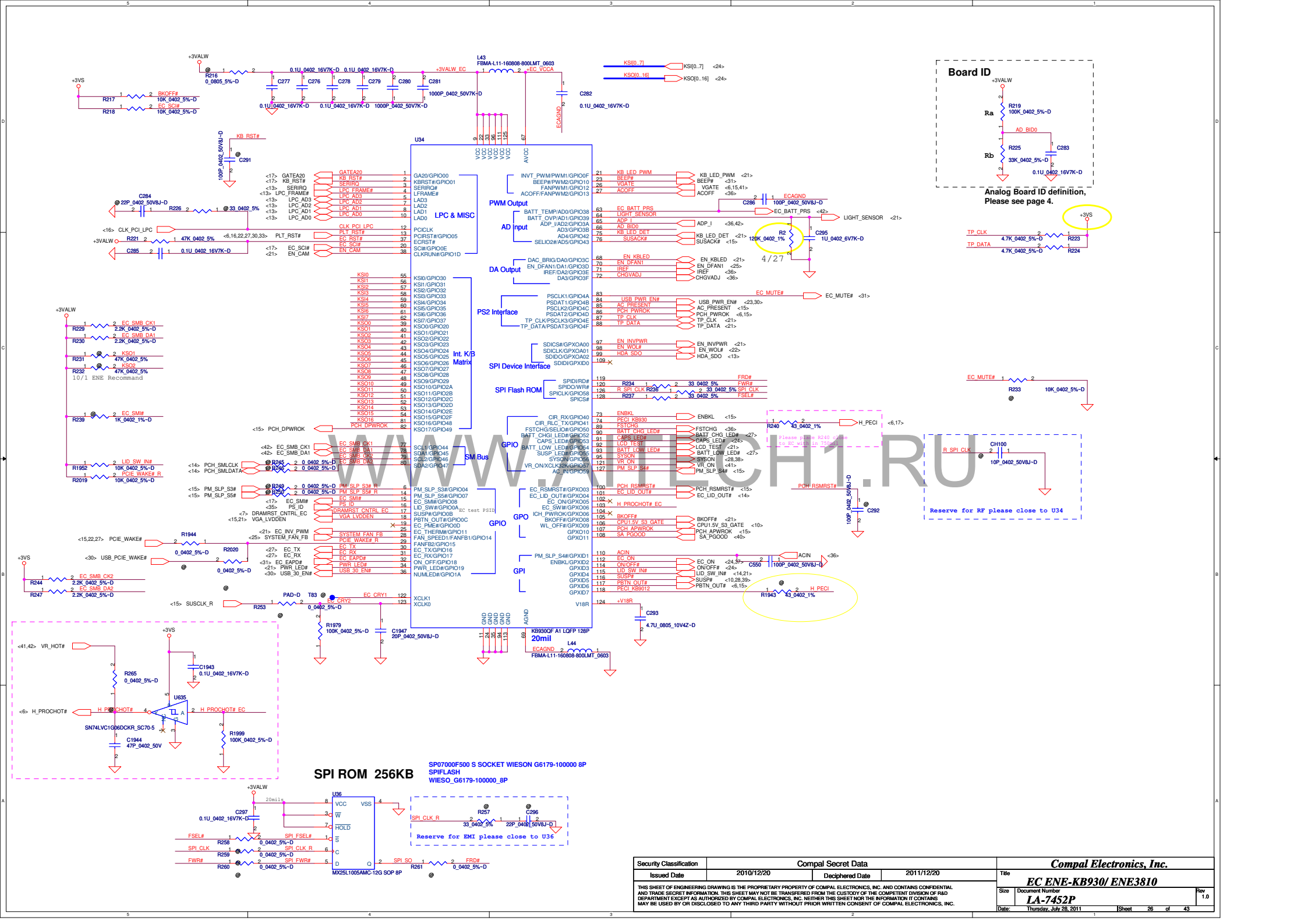


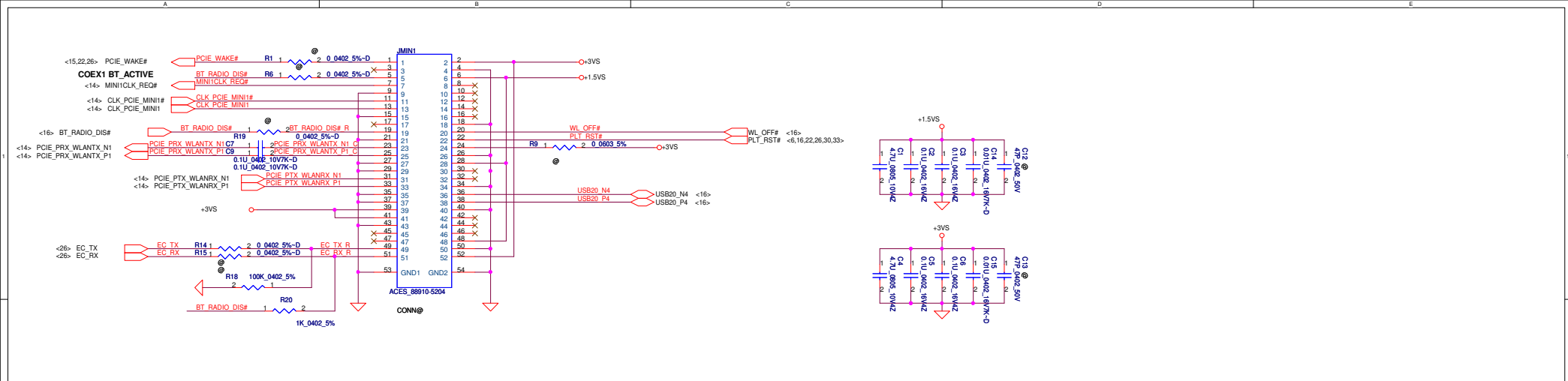
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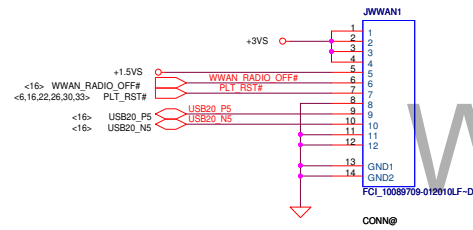
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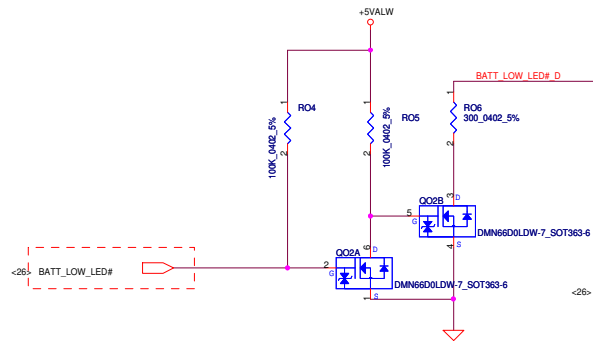


TO WWAN BOARD

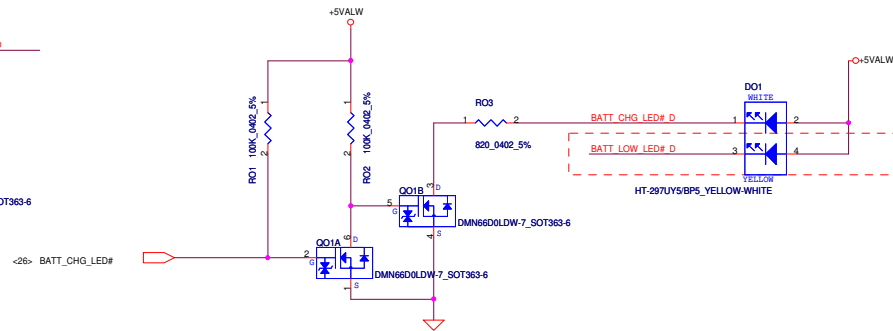


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BATT LOW

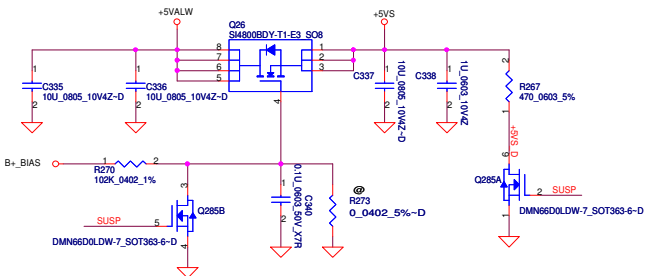


BATT CHARGE

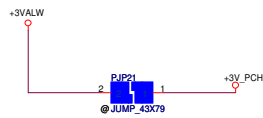


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				Size	Document Number
				LA-7452P	
				Date	Thursday, July 28, 2011
				Sheet	27 of 43
				Rev	1.0

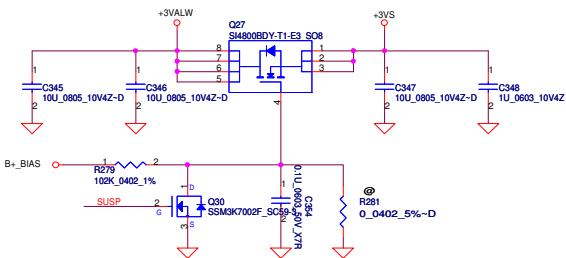
+5VALW to +5VS



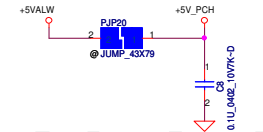
+3VALW to +3V_PCH



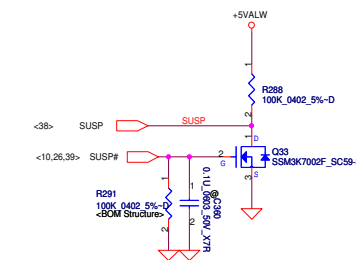
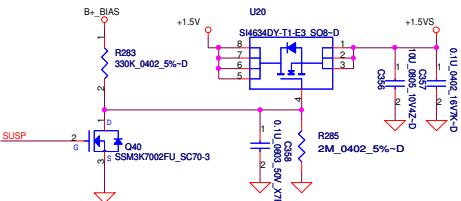
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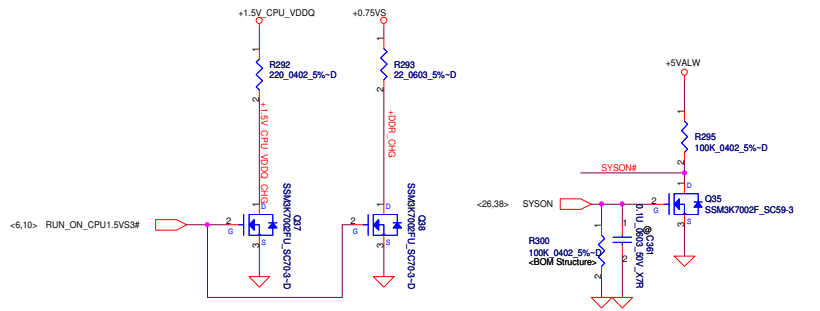
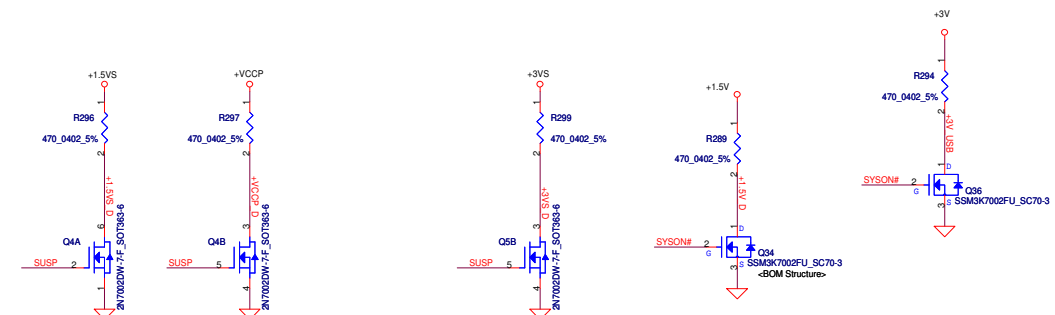
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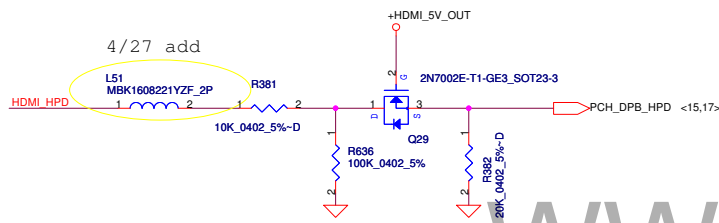
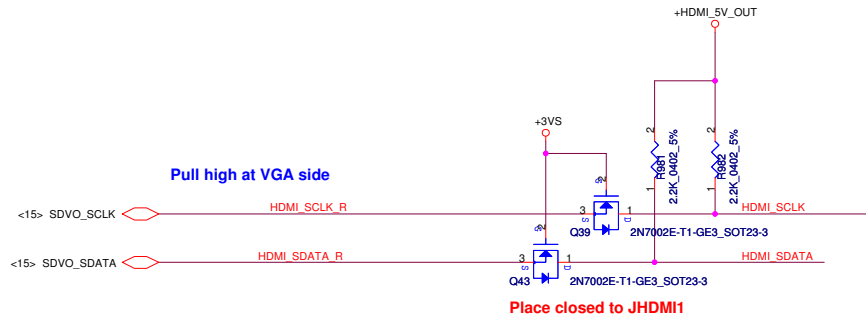
+1.5V To +1.5VS



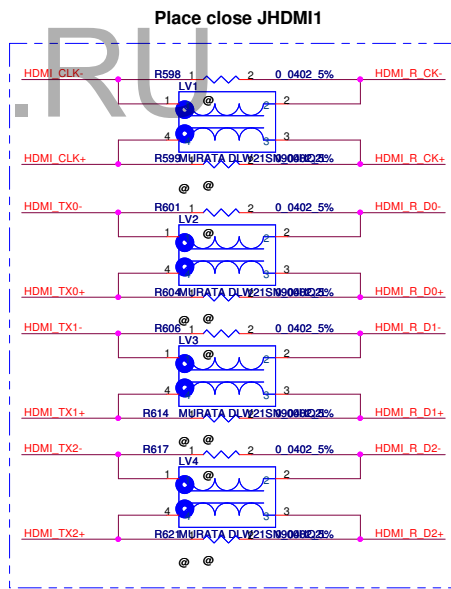
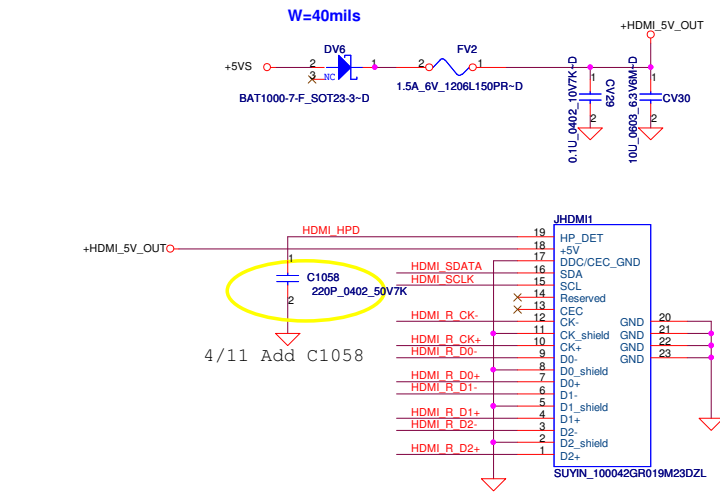
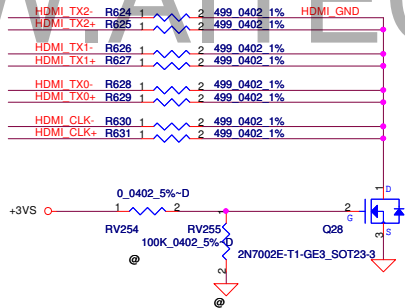
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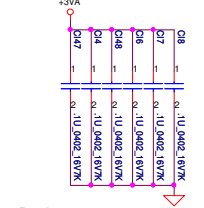
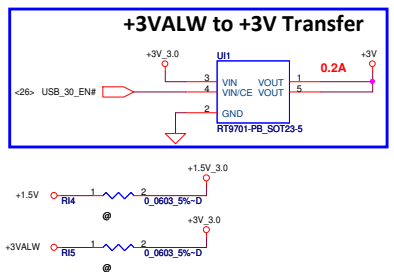
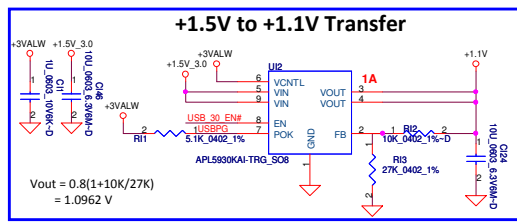
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Issued Date	2010/12/20	Deciphered Date	2011/12/20	Title DC/DC Interface	
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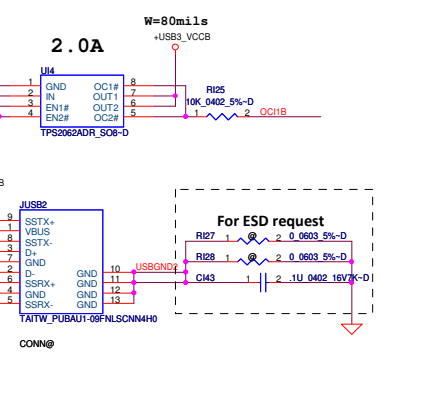
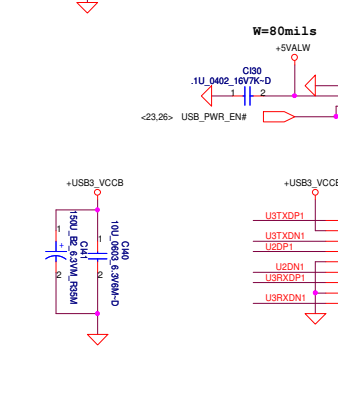
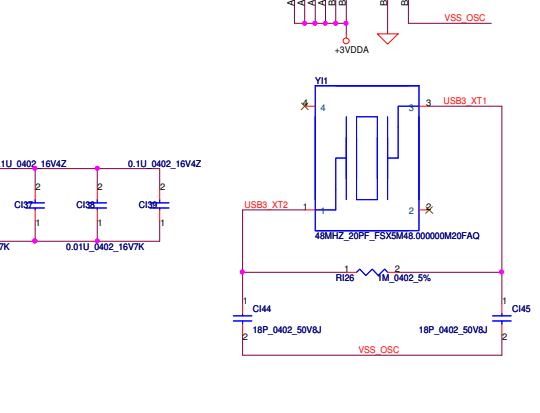
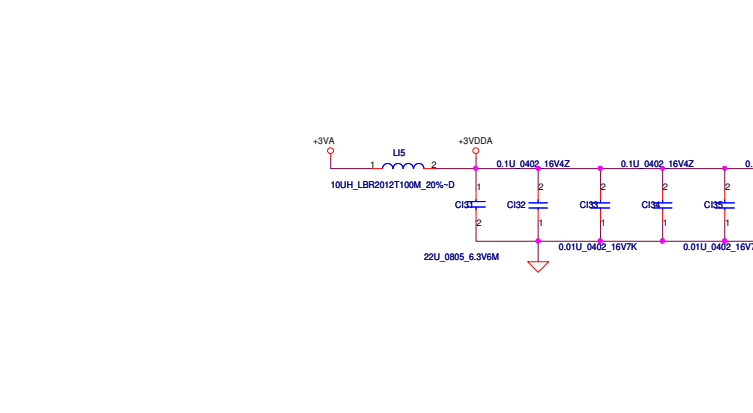
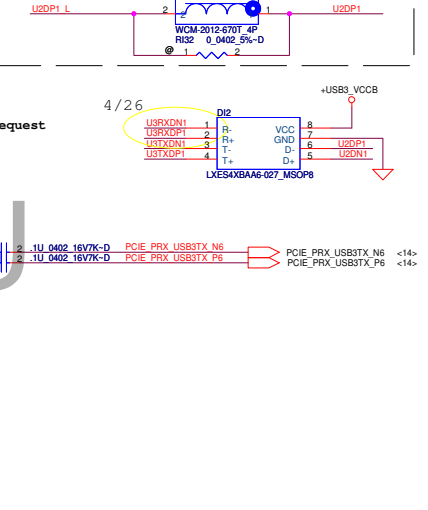
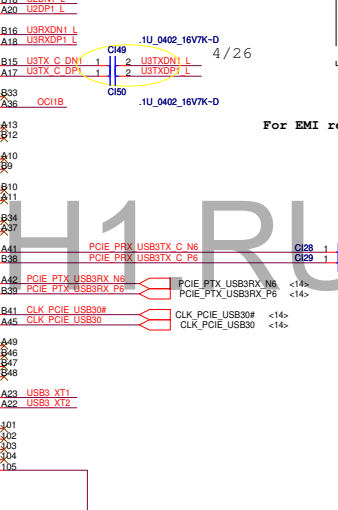
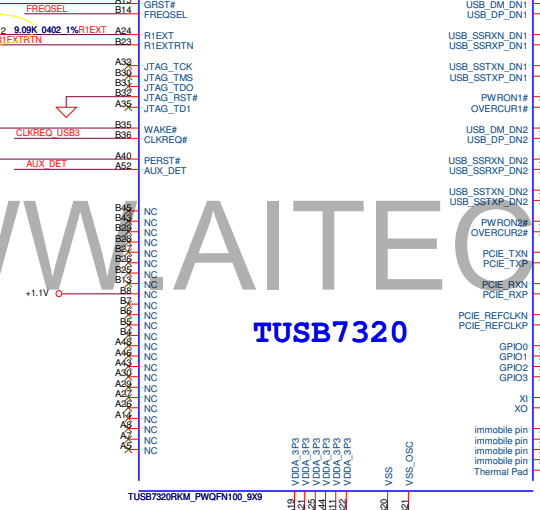
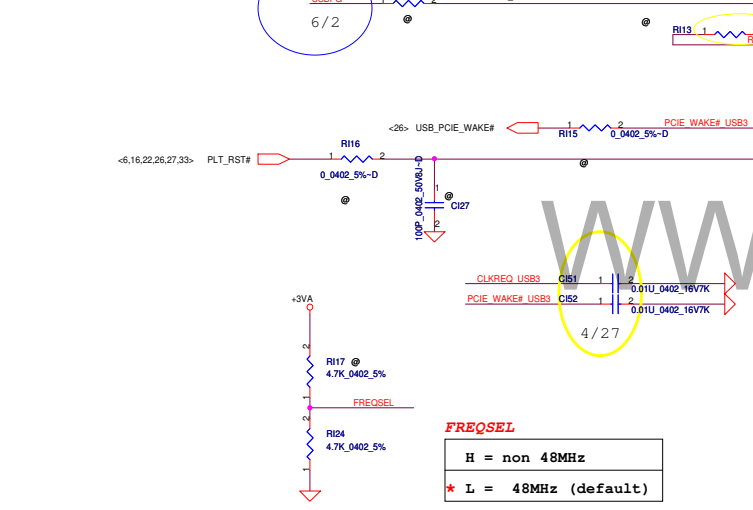
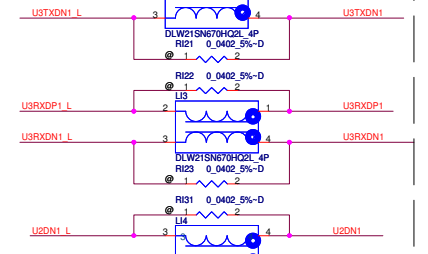
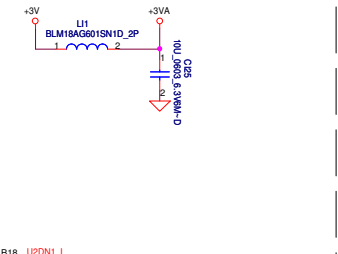
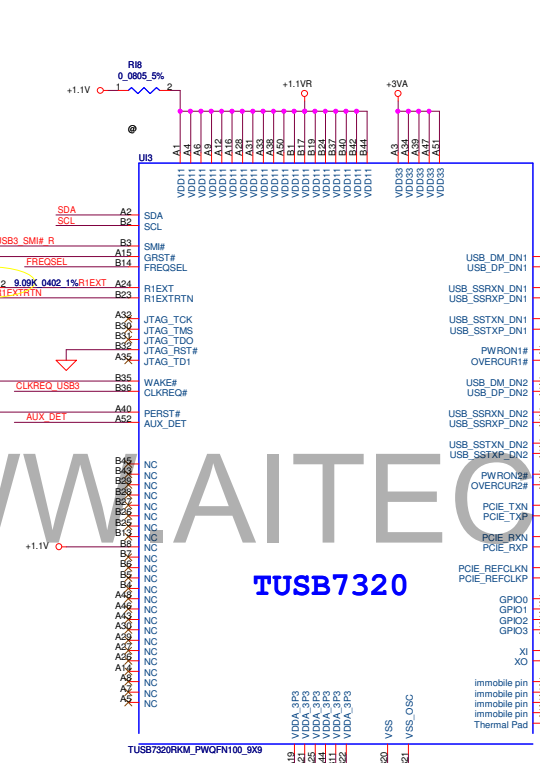
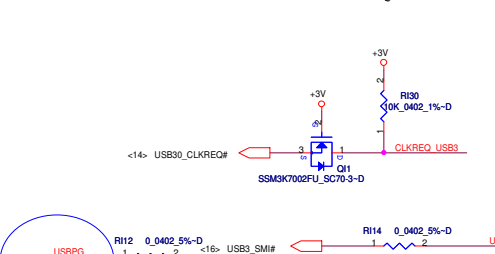
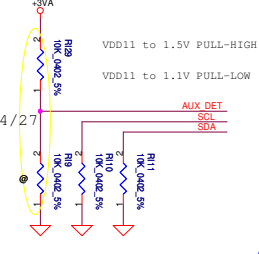
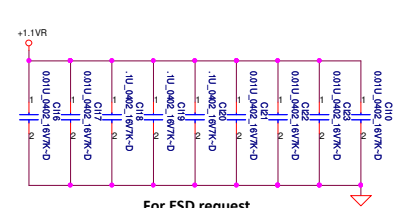
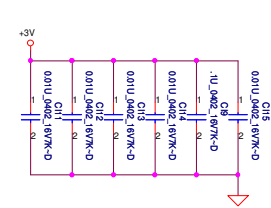
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<15> PCH_DPB_N1	C631	2	1	0.1U 0402 16V7K	HDMI TX1-
<15> PCH_DPB_P1	C632	2	1	0.1U 0402 16V7K	HDMI TX1+
<15> PCH_DPB_N2	C633	2	1	0.1U 0402 16V7K	HDMI TX0-
<15> PCH_DPB_P2	C634	2	1	0.1U 0402 16V7K	HDMI TX0+
<15> PCH_DPB_N3	C635	2	1	0.1U 0402 16V7K	HDMI CLK-
<15> PCH_DPB_P3	C636	2	1	0.1U 0402 16V7K	HDMI CLK+

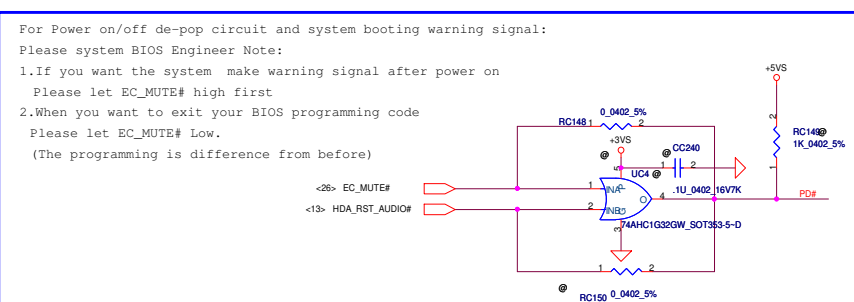
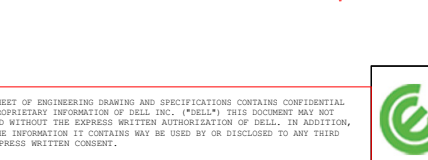
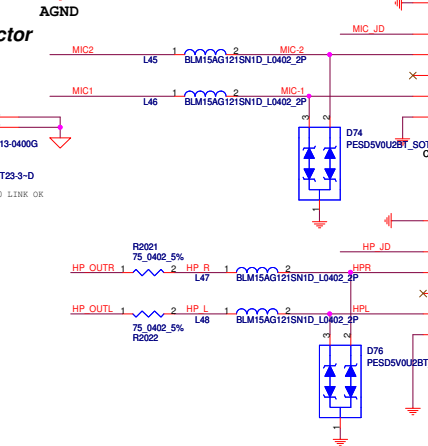
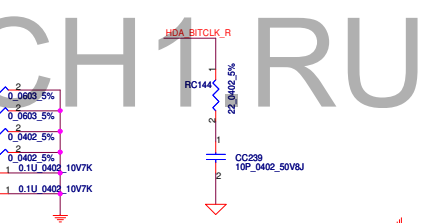
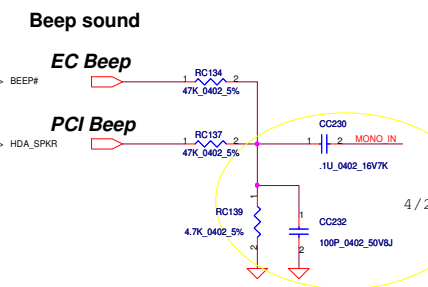
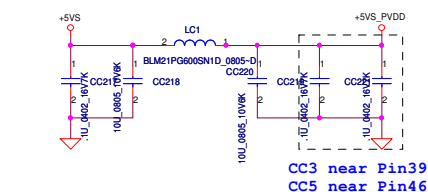
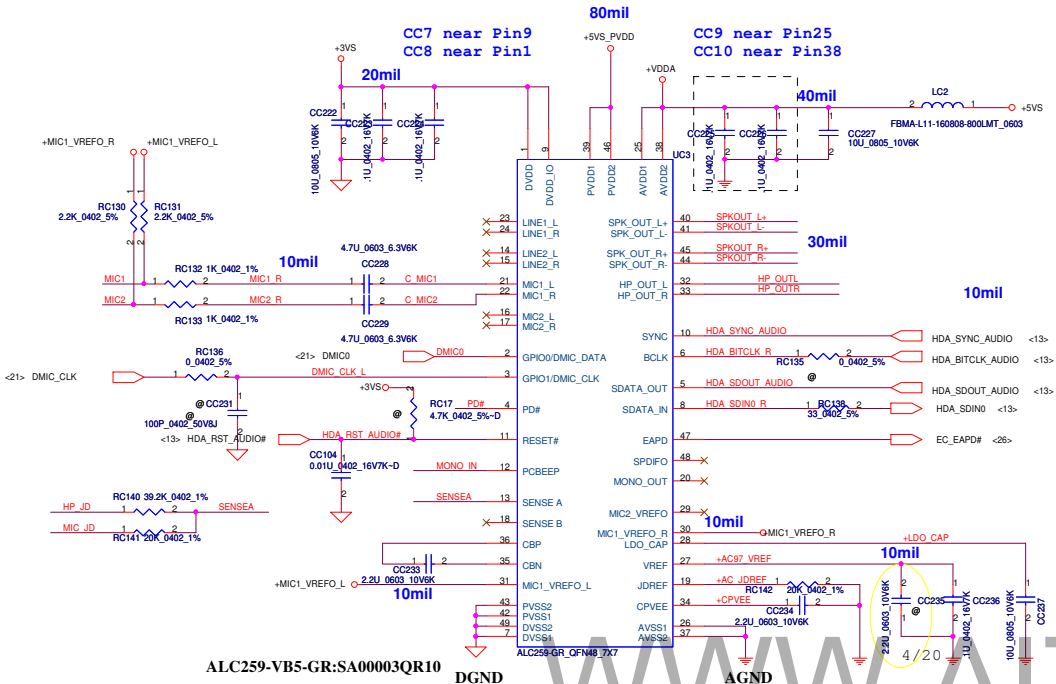


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				Size Document Number Custom LA-7452P
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7K for customer request, can use other kind of capacitor, like Y5V.





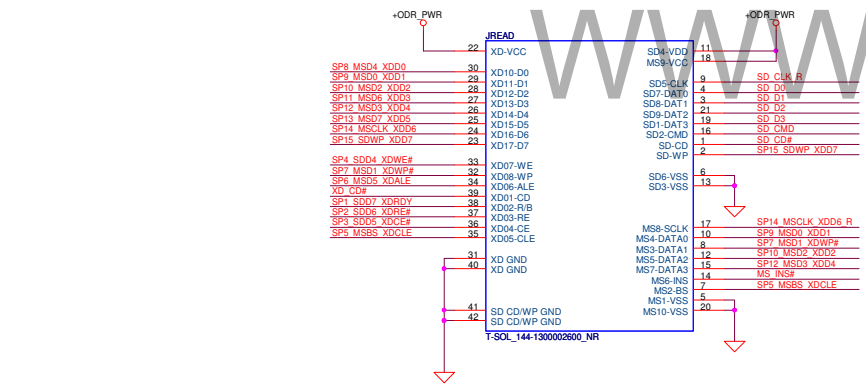
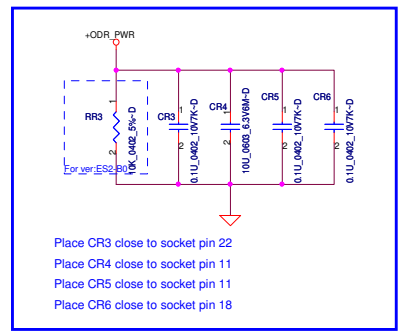
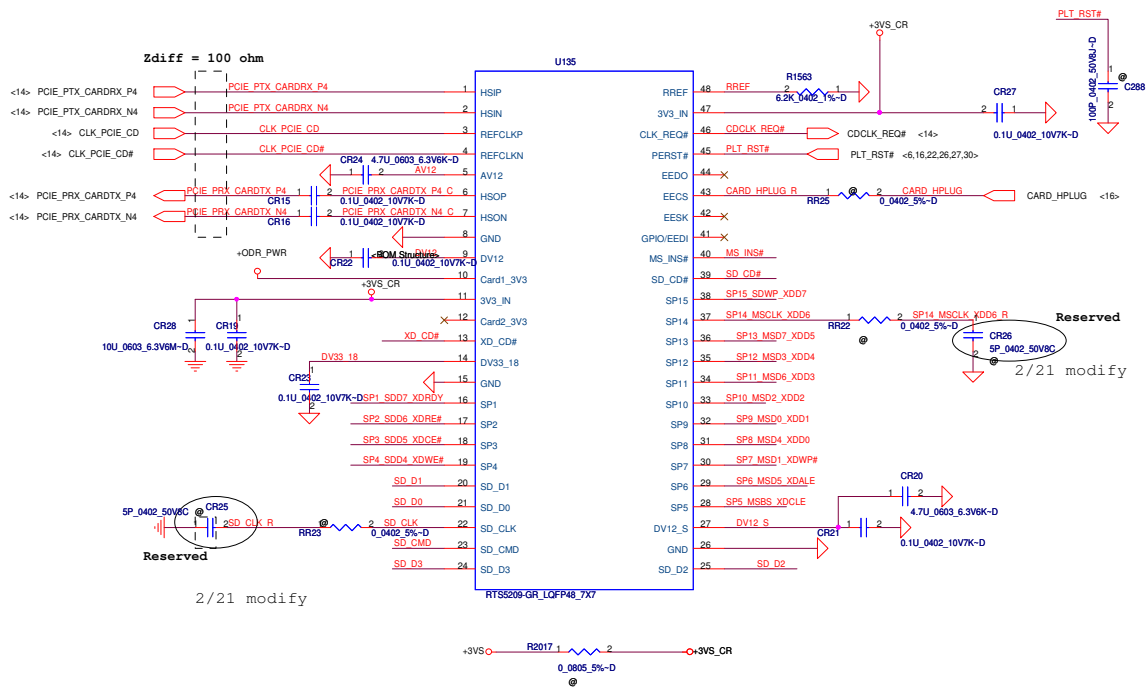
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[illegible]

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<15> DISP_A0P_VGA	C1070_2	1	0.1U	0402	106K-D	DISP_C_A0P
<15> DISP_A1N_VGA	C1071_2	1	0.1U	0402	106K-D	DISP_C_A1N
<15> DISP_A1P_VGA	C1073_2	1	0.1U	0402	106K-D	DISP_C_A1P
<15> DISP_A2N_VGA	C1072_2	1	0.1U	0402	106K-D	DISP_C_A2N
<15> DISP_A2P_VGA	C1074_2	1	0.1U	0402	106K-D	DISP_C_A2P
<15> DISP_A3N_VGA	C1075_2	1	0.1U	0402	106K-D	DISP_C_A3N
<15> DISP_A3P_VGA	C1076_2	1	0.1U	0402	106K-D	DISP_C_A3P



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				mini DP		
				Size	Document Number	Rev
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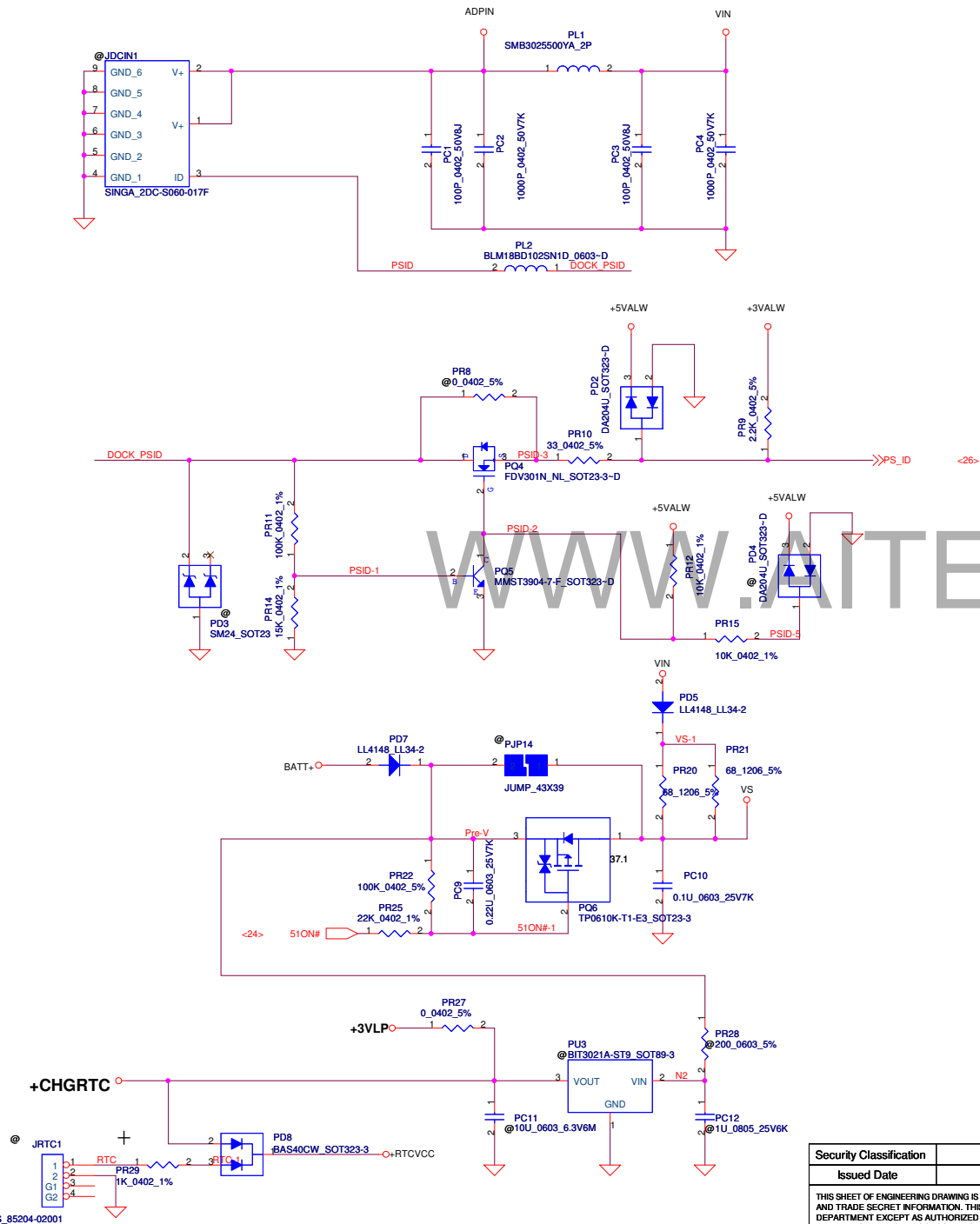
Version change list (P.I.R. List)

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Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	KB930A TO KB9012					
2						
3						
4						
5						
6						
7						
8						
9						
10						

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				Custom		1.0
Date: Thursday, July 28, 2011				Sheet	34 of 43	

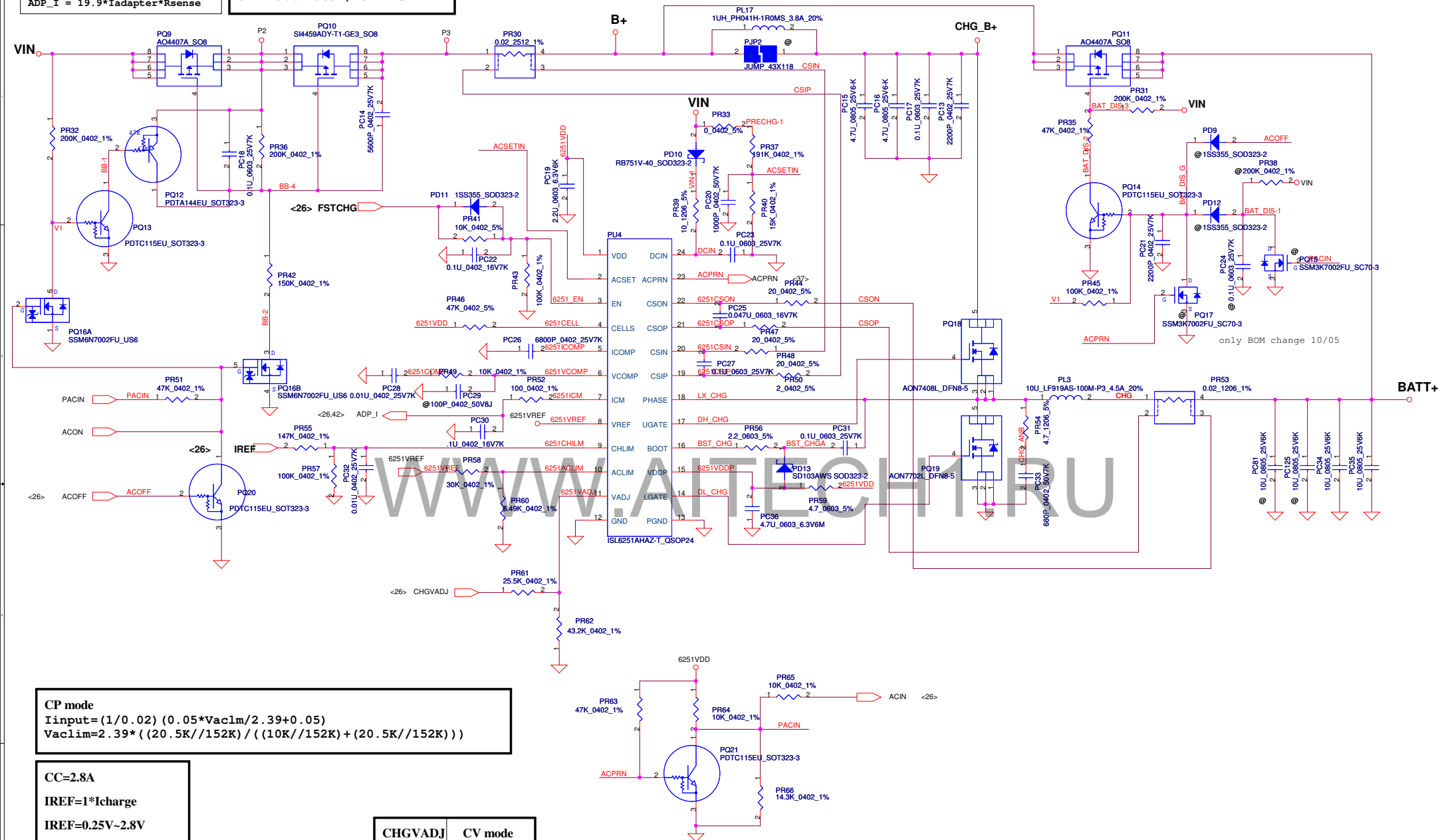


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				Size	Document Number		Rev
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Iada=0~3.333A (65W/19.5V=3.333A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 3A



CP mode

$I_{input} = (1/0.02) (0.05 \cdot V_{acim} / 2.39 + 0.05)$
 $V_{acim} = 2.39 \cdot ((20.5K / 152K) / ((10K / 152K) + (20.5K / 152K)))$

CC=2.8A

$I_{REF} = 1 \cdot I_{charge}$
 $I_{REF} = 0.25V - 2.8V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

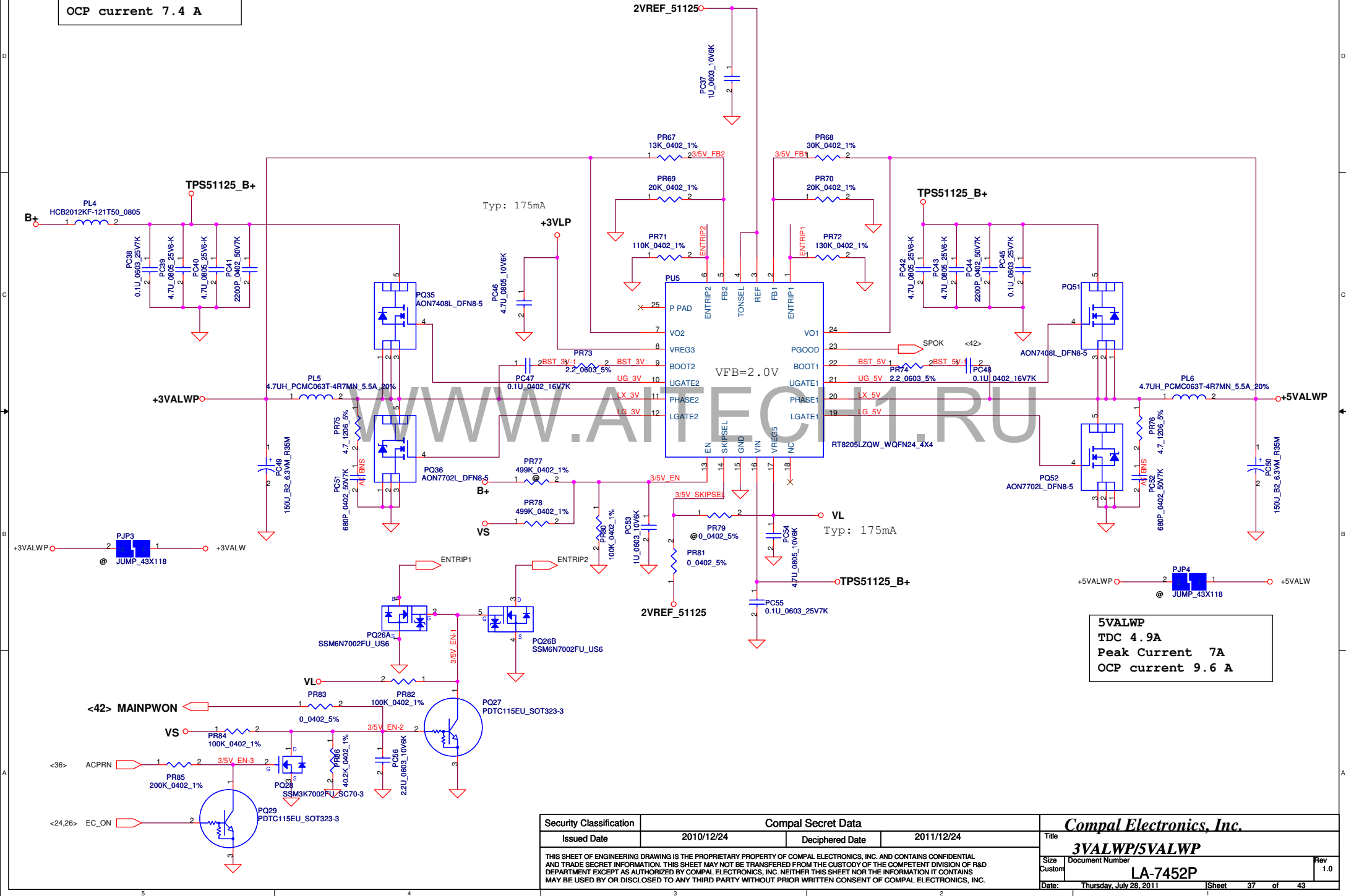
CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

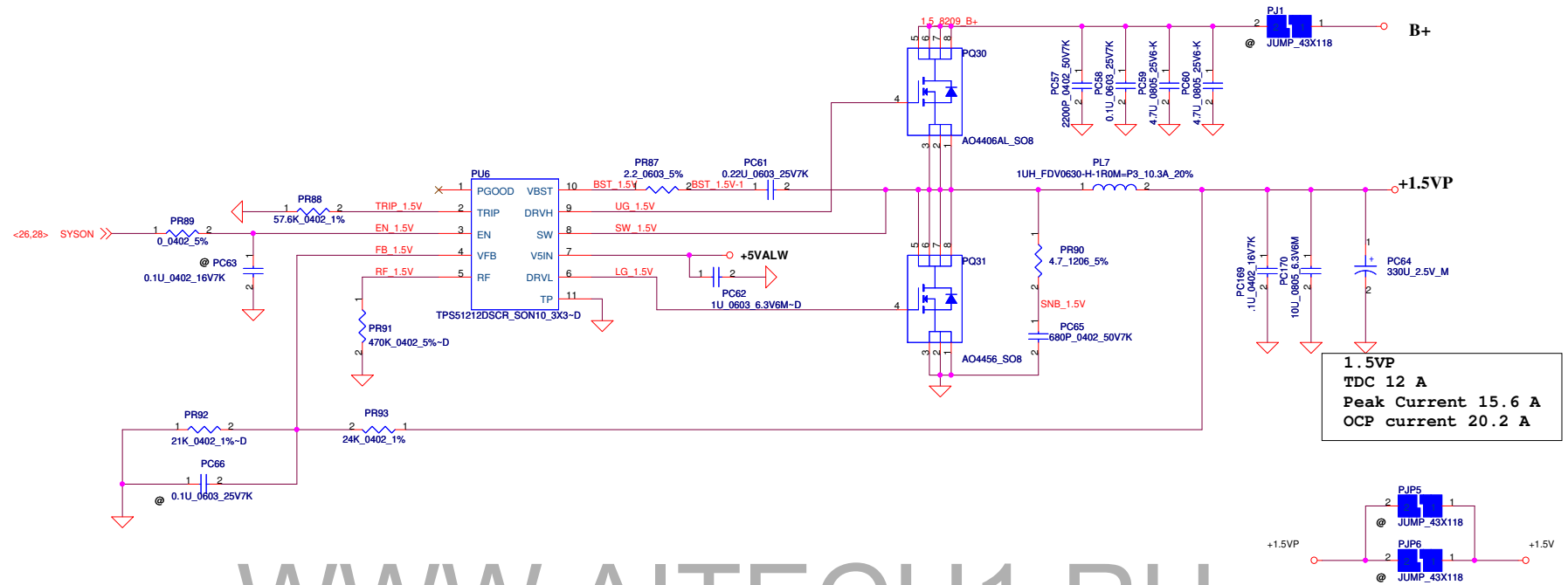
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Issued Date	2010/12/24	Deciphered Date	2011/12/24	Compal Electronics, Inc.
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3.3VALWP
TDC 4.02 A
Peak Current 5.7A
OCP current 7.4 A

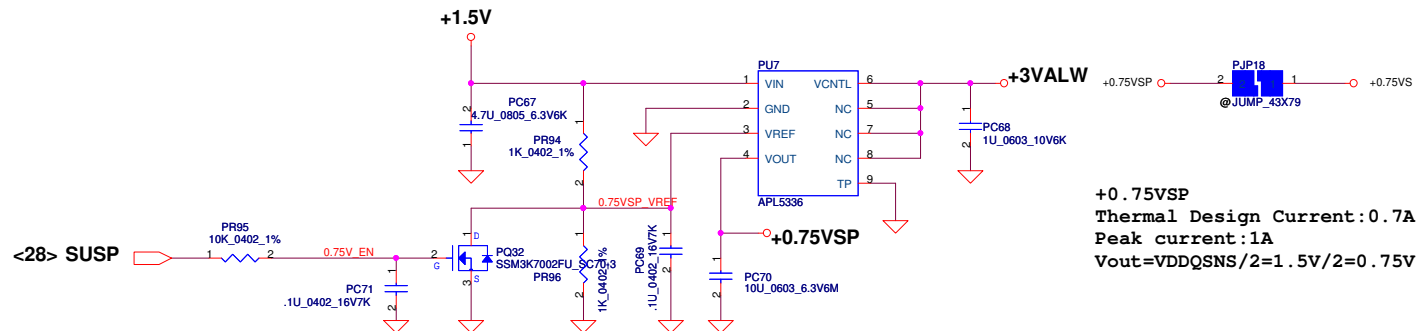
5VALWP
TDC 4.9A
Peak Current 7A
OCP current 9.6 A

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Issued Date	2010/12/24	Deciphered Date	2011/12/24	Title	3VALWP/5VALWP
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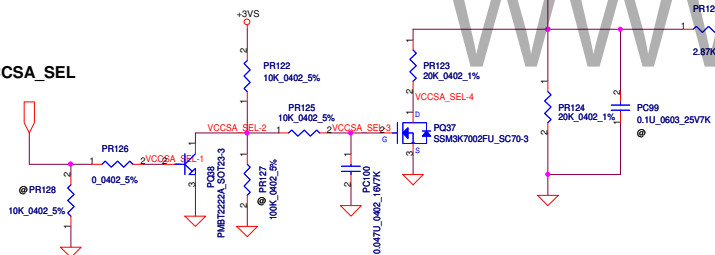


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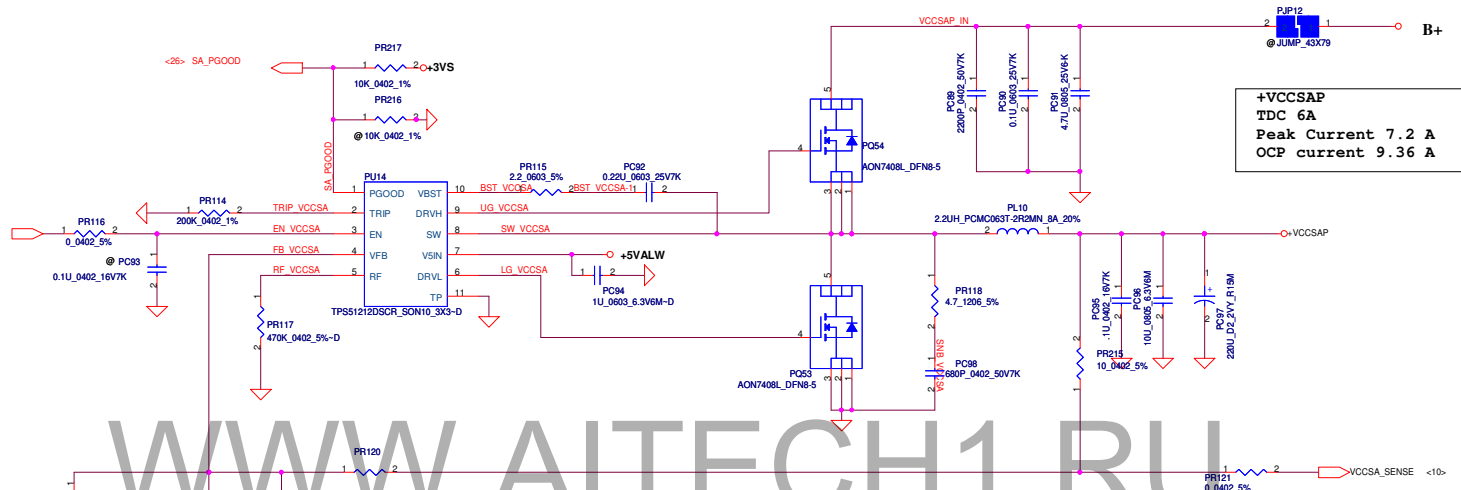


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<10> VCCSA_SEL

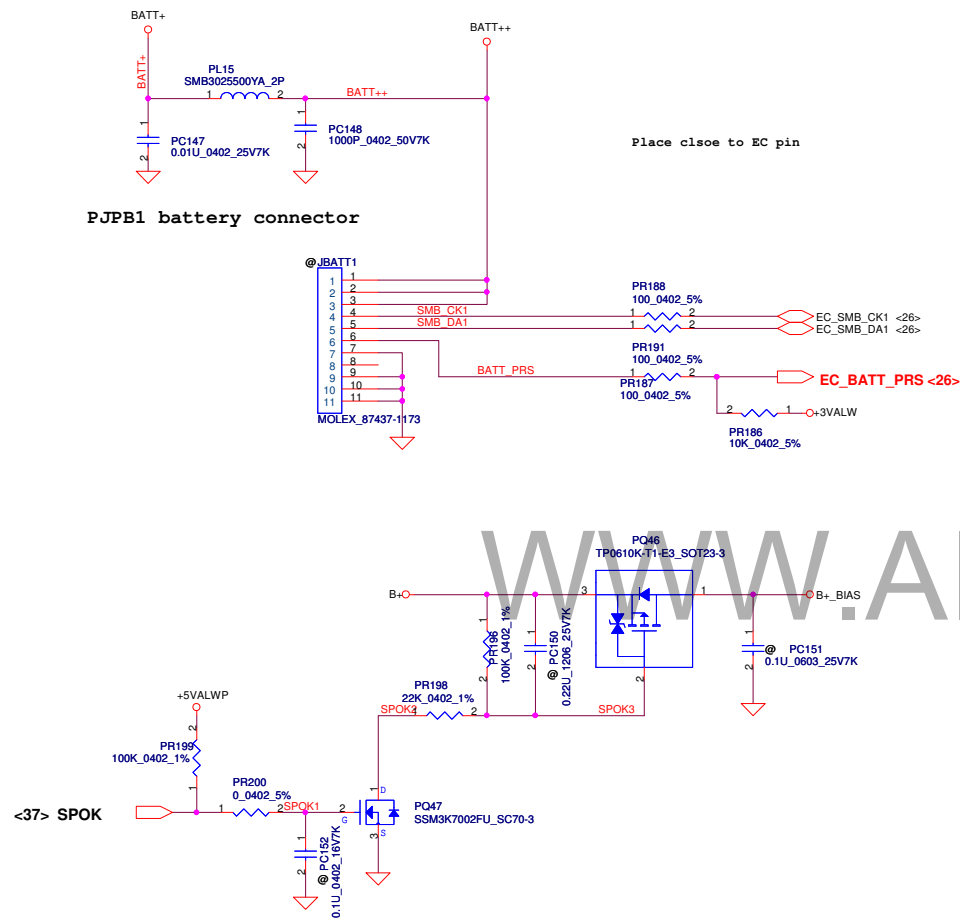


<39> VTPWRGOOD



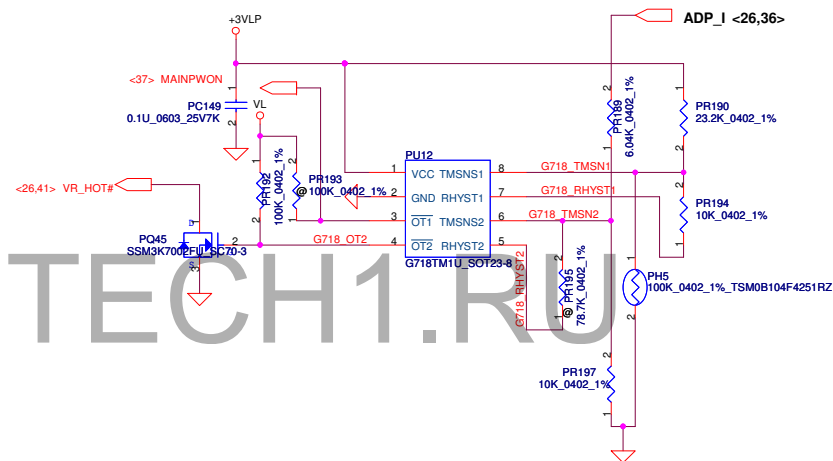
+VCCSAP
TDC 6A
Peak Current 7.2 A
OCP current 9.36 A

VCCSA_SEL	VCCSA Vout	Required on 2011 / 2012	Required
0	0.9V	Yes / Yes	
1	0.8V	Yes / Yes	



Battery Connect/OTP

PH3 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



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Version change list (P.I.R. List)

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Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	modify Vcore and GFX boost resistance		P46	change PR136,PR163,PR179 to 2.2 +-5% 0603.	2011.2.10	before SSI
2	modify 1.5V Enable signal		P43	change PR81 connect to SYSON.	2011.3.24	SSI
3	integrate mosfet		P45	change PQ53 PQ54 to AON7408L		
4	modify Vcore and GFX's loadline and OCP		P46	change PC137 to .033U 16V K X7R 0402 change PR171 to 1.65K +-1% 0402 change PR149 to 1.33K +-1% 0402 change PR131 to 3.24K +-1% 0402		
5	integrate mosfet		P43 P45	change PQ32 to SSM3K7002FU 1N SC70-3 change PQ37 to SSM3K7002FU 1N SC70-3		
6	add capacitance for RF team suggest item		P41 P43 P44	change PC81 PC125 to 10U 25V K X5R 0805 H1.25 change PC169 to .1U 16V K X7R 0402 change PC170 to 10U 6.3V M X5R 0805 H1.25 change PC171 to .1U 16V K X7R 0402 change PC172 to 10U 6.3V M X5R 0805 H1.25		
7	modify 1.5V OCP resistance		P43	change PR88 to 57.6K +-1% 0402		
8	modify VCCP OCP resistance		P44	change PR100 to 80.6K +-1% 0402		
9	modify choke footprint for DFX requirement			change PL5,PL6,PL7,PL8,PL10 to TAI-T_VMPI0703AR-100M-Z01_2P		
10	modify PQ11 Vgs resistance		P41	change PR31 to 200K +-1% 0402 change PR35 to 47K +-1% 0402		
11	modify net name SPOK-'		P47	change the net name of PQ47 pin2 to SPOK1 change the net name of PQ47 pin1 to SPOK2 change the net name of PQ46 pin2 to SPOK3		
12	modify PU12 vcc power from +3VALW to +3VLP		P47	change PR190.1 to +3VLP change PR149.1 to +3VLP change PU12.1 to +3VLP		
13	modify OTP resistance		P47	change PR190 to 23.2K +-1% 0402 change PR194 to 10K +-1% 0402		
14	modify VCORE VCCP resistance		P46	change PR145 to 1 +-5% 0603		

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